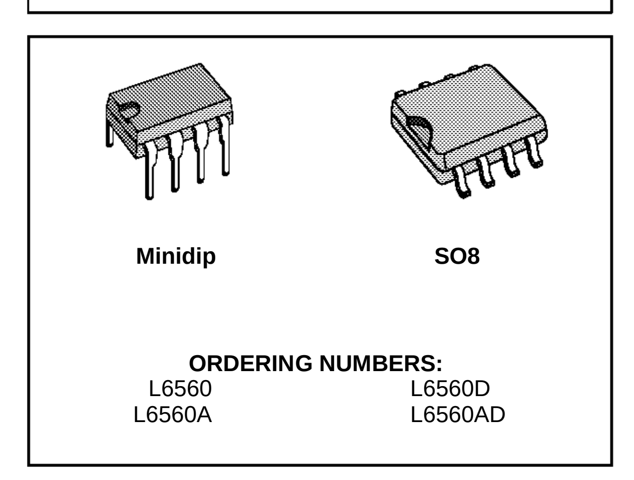
L6560
L6560A

POWER FACTOR CORRECTOR

ADVANCE DATA

- VERY PRECISE ADJUSTABLE INTERNAL OUTPUT OVERVOLTAGE PROTECTION
- HYSTERETIC START-UP ($I_{START-UP}$ < 0.5mA)
- VERY LOW QUIESCENT CURRENT (< 3.5mA)
- INTERNAL START-UP TIMER
- TRANSITION MODE OPERATING
- TOTEM POLE OUTPUT CURRENT: ±400mA
- DIP8/SO8 PACKAGES

MULTIPOWER BCD TECHNOLOGY



ORDERING NUMBERS:

L6560	L6560D
L6560A	L6560AD

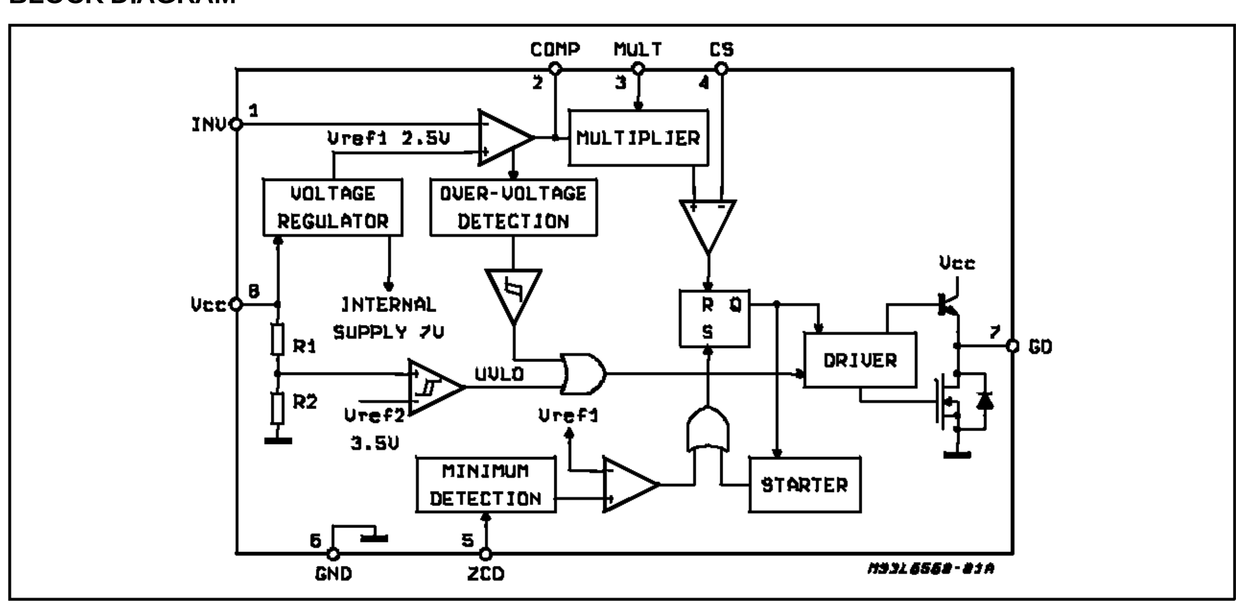
DESCRIPTION

The L6560/A is a monolithic integrated circuit in Minidip and SO8 packages, designed as a controller and driver of a discrete power MOS transistor for the implementation of active power factor correction, for sinusoidal line current consumption.

Realized in mixed BCD technology, the chip integrates:

- An undervoltage lockout with micropower start-up and hysteresis
- An internal temperature compensated precise band gap reference
- A stable error amplifier
- One quadrant multiplier
- Current sense comparator
- An output overvoltage protection circuit
- A totem-pole output stage able to drive a POWER MOS or IGBT devices with source and sink current of 400mA. The chip works in transition mode and is particularly intended for lamp ballast applications and for low power SMPS.

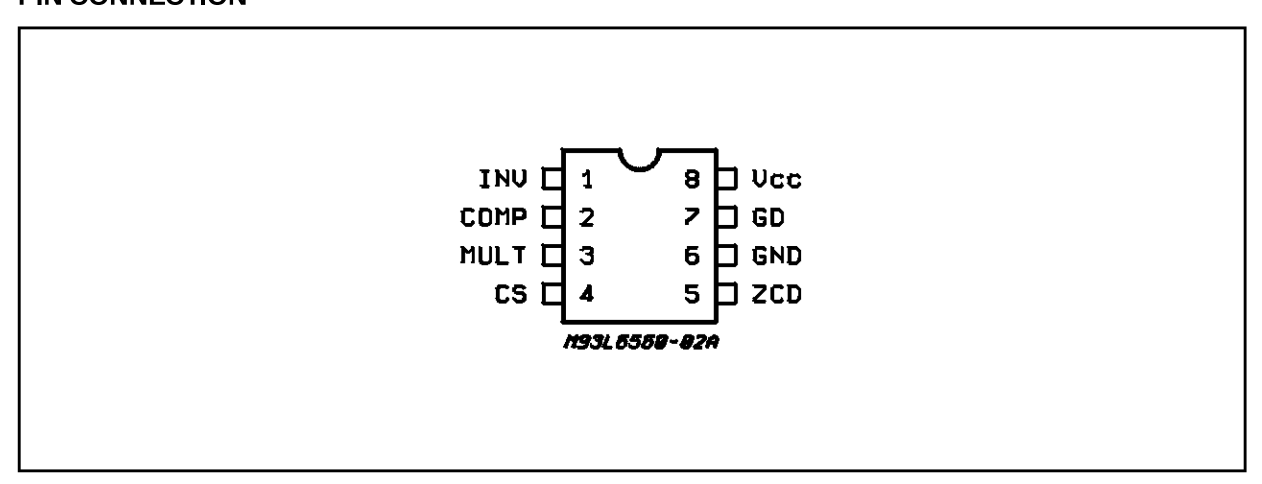
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Pin	Parameter	Value	Unit
I_{VCC}	8	$I_{CC} + I_Z$	30	mA
I_{GD}	7	Output Totem Pole Peak Current (2μs)	±700	mA
INV, COMP MULT	1, 2, 3	Analog Inputs & Outputs	-0.3 to 7	V
CS	4	Current Sense Input	-0.3 to 7	V
ZCD	5	Zero Current Detector	5 (source) 10 (sink)	mA mA
P_{tot}		Power Dissipation @T_{amb} = 50 °C **(Minidip)** **(SO8)**	1 0.65	W
T_j		Junction Temperature Operating Range	-25 to 150	°C
T_{stg}		Storage Temperature	-55 to 150	°C

PIN CONNECTION



THERMAL DATA

Symbol	Parameter	SO 8	MINIDIP	Unit
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	150	100	°C/W

PIN FUNCTIONS

N.	Name	Function
1	INV	Inverting input of the error amplifier. A resistive divider is connected between output regulated voltage and this point, to provide the voltage feedback.
2	COMP	Output of error amplifier. A feedback compensation network is placed between this pin and the INV pin.
3	MULT	Input of the multipler stage. A resistive divider connects to this pin the rectified mains. A voltage signal, proportional to the rectified mains, appears on this pin.
4	CS	Input to the comparator of the control loop. The current is sensed by a resistor and the resulting voltage is applied to this pin.
5	ZCD	Zero current detection input.
6	GND	Ground of the control section.
7	GD	Gate driver output. A push pull output stage is able to drive the Power MOS with peak current of 400mA (source and sink).
8	V_{CC}	Supply voltage of driver and control circuits.



ELECTRICAL CHARACTERISTICS (V_{CC} = 14.5V; T_j = 25°C unless otherwise specified)

SUPPLY VOLTAGE SECTION

Symbol	Pin	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{CC}	8	Operating Range	after turn-on	11		18	V
$V_{CC\ ON}$	8	Turn-on Threshold	**L6560** **L6560A**	13.5 11	14.5 12	15.5 13	V v
$V_{CC\ OFF}$	8	Turn-off Threshold	**L6560** **L6560A**	9 8.7	10 9.6	11 10.5	V V
Hys	8	Hysteresis	**L6560** **L6560A**	4.3 2.5	4.7 2.8	5.1 3.1	V V

SUPPLY CURRENT SECTION

Symbol	Pin	Parameter	Test Condition	Min.	Typ.	Max.	Unit
$I_{START-U}$	8	Start-up Current	before turn-on at: V_{CC} = 13V (L6560) V_{CC} = 10.5V (L6560A)		0.3	0.5	mA
I_{CC}	8	Operating Supply Current	C_L = 0nF @ 70KHz		2.5	3.5	mA
			C_L = 1nF @ 70KHz		3.2	4	mA
			in OVP condition V_{pin1} = 2.7V		0.9	1.3	mA
V_Z	8	Zener Voltage	I_{CC} = 25mA	18	20	22	V

ERROR AMPLIFIER SECTION

Symbol	Pin	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{INV}	1	Voltage Feedback Input Threshold		2.46	2.5	2.54	V
			$-25 \leq T_J \leq 85°C$; $12V < V_{CC} < 18V$	2.43		2.56	
T_S		Temperature Stability	T_{amb} = -25 to 85°C		0.5		%
R_L		Line Regulation	V_{CC} = 11 to 18V		1	4	mV
I_{INV}	1	Input Bias Current			0.1	1	µA
G_V		Voltage Gain	Open loop	60	80		dB
I_{COMP}	2	Source Current ($V_1 < V_{ref}$)	V_{COMP} = 5V	0.14	0.2		mA
		Sink Current ($V_1 > V_{ref}$)		0.5	1		mA

MULTIPLIER SECTION

Symbol	Pin	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{MULT}	3	Operating Voltage		0 to 2.5	0 to 4.2		V
$\frac{\Delta V_{CS}}{\Delta V_{mult}}$		Output Max. Slope	V_{MULT} = from 0V to 1V V_{COMP} = 6V	0.9	1.25	1.6	
K		Gain	V_{MULT} = 1V V_{COMP} = 5V	0.45	0.65	0.85	1/V

CURRENT SENSE COMPARATOR

Symbol	Pin	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{CS}	4	Voltage Threshold	V_{MULT} = 2.5V V_{COMP} = 6V	1.6		1.9	V
I_{CS}	4	Input Bias Current				5	µA
$t_{d\ (H-L)}$	4	Delay to Output			200	400	ns



ELECTRICAL CHARACTERISTICS (continued)

ZERO CURRENT DETECTOR

Symbol	Pin	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{ZCD}	5	Input Threshold Voltage Rising Edge		1.8		2.3	V
		Hysteresis		0.3	0.5	0.7	V
V_{ZCD}	5	Clamp Voltage	I_{ZCD} = 3mA	5	5.7	6.4	V
V_{ZCD}	5	Clamp Voltage	I_{ZCD} = –3mA	0.4	0.7	1	V

OUTPUT SECTION

Symbol	Pin	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{GD}	7	Dropout Voltage	$I_{GDsource}$ = 200mA		1.2	2	V
			$I_{GDsource}$ = 20mA		0.7	1	V
			I_{GDsink} = 200mA			1.5	V
			I_{GDsink} = 20mA			0.3	V
t_r	7	Output Voltage Rise Time	CL = 1nF		50	120	ns
t_f	7	Output Voltage Fall Time	CL = 1nF		40	100	ns

OUTPUT OVERVOLTAGE SECTION

Symbol	Pin	Parameter	Test Condition	Min.	Typ.	Max.	Unit
I_{OVP}	2	OVP Triggering Current		36	40	44	µA

RESTART TIMER

Symbol	Pin	Parameter	Test Condition	Min.	Typ.	Max.	Unit
t_{START}		Start Timer		45	60		µs

OVER VOLTAGE PROTECTION OVP

The output voltage is expected to be kept by the operation of the PFC circuits close to its reference value that is set by the ratio of the two external resistors R_1 and R_2 (see fig. 2), taking into consideration that the non inverting input of the error amplifier is biased inside the L6560 at 2.5V.

In steady state conditions, the current through R1 and R2 is:

$$I_{SC} = \frac{\Delta V_{outsc} - 2.5}{R1}$$

$$\text{or} \quad I_{SC} = \frac{2.5}{R2}$$

and, if the external compensation network is made only with a capacitor C, the current through C is equal zero.

When the output voltage increases abruptly the current through R1 becomes:

$$I_{R1} = \frac{V_{out} - 2.5}{R1}$$

$$I_{R1} = \frac{V_{outsc} + \Delta V_{OUT} - 2.5}{R1} = I_{sc} + \Delta I.$$

Since the current through R2 doesn't change, the ΔI current must flow through the capacitor C and enter in the error amplifier.

This current is mirrored inside the L6560, and compared with a precise internal reference of 40µA. Whenever such 40µA limit is exceed, the OVP protection is triggered (Dynamic OVP), and the external power transistor is switched off, until the overvoltage situation disappears. However if the overvoltage persists, before that the transient condition of dynamic circuit exhausts, an internal comparator (Static OVP) latches the OVP condition keeping the external power switch turned off (see fig. 1).

The OVP value is threfore set by the equation $OVP = \Delta Vout = R_1 \cdot 40\mu A$.

Typical values for R_1, R_2 and C are reported in the application circuit. The overvoltage can be set independently from the average output voltage. The precision in setting the overvoltage threshold is 7% of the overvoltage value (for instance $\Delta V = 60V \pm 4.2V$).

Figure 1.

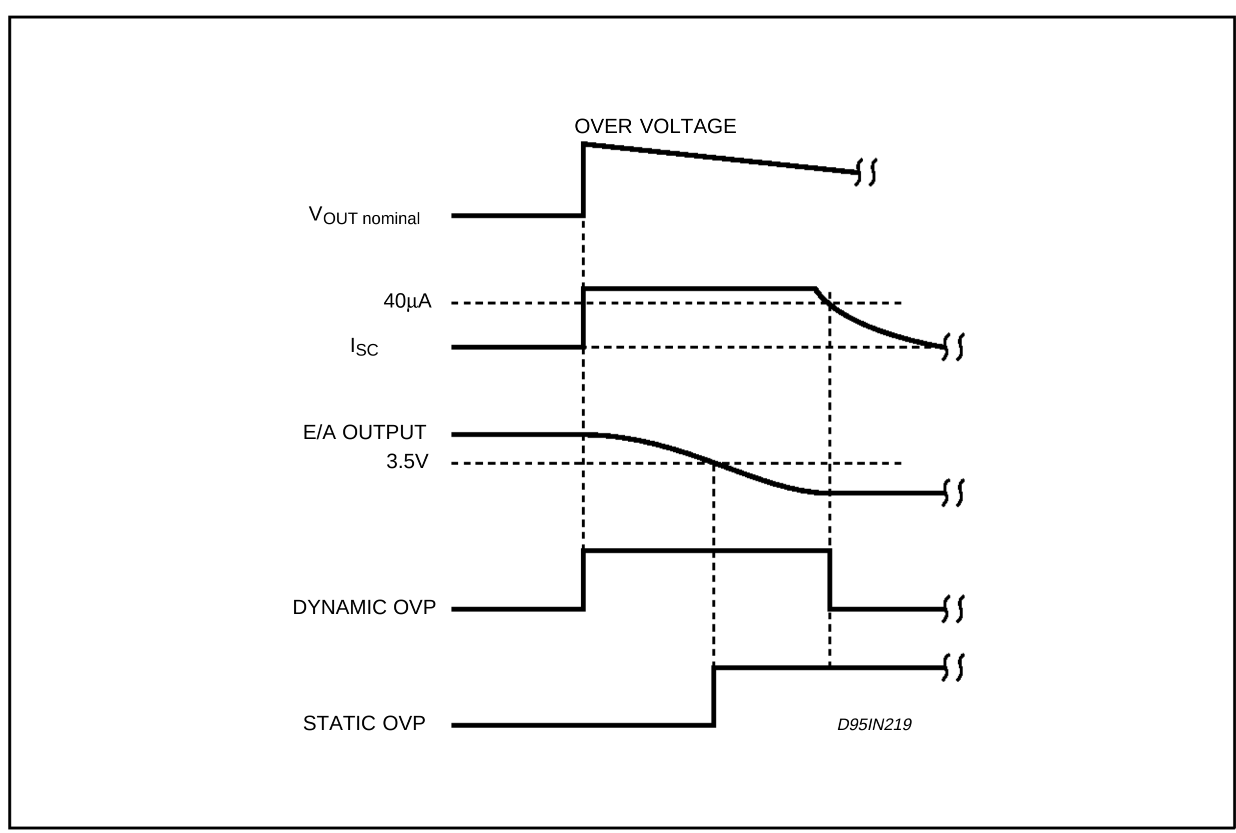


Figure 2: Overvoltage Protection Circuit

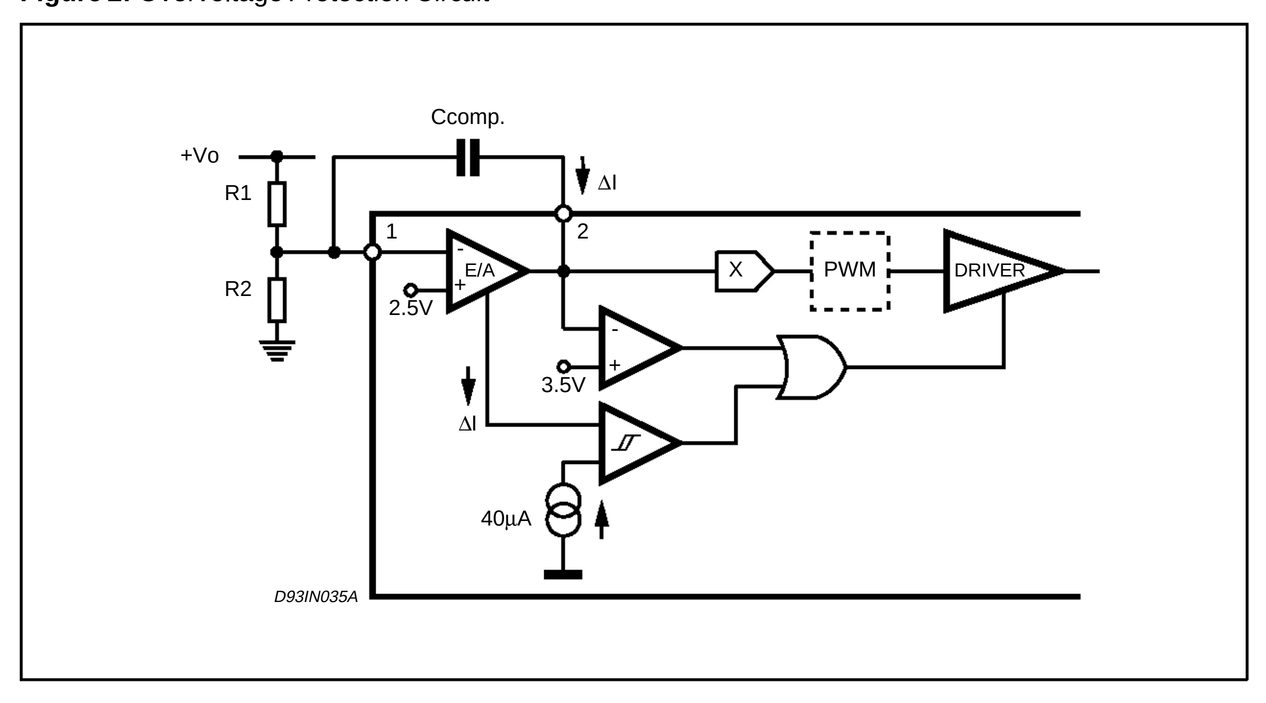


Figure 3: Typical Application Circuit (100W)

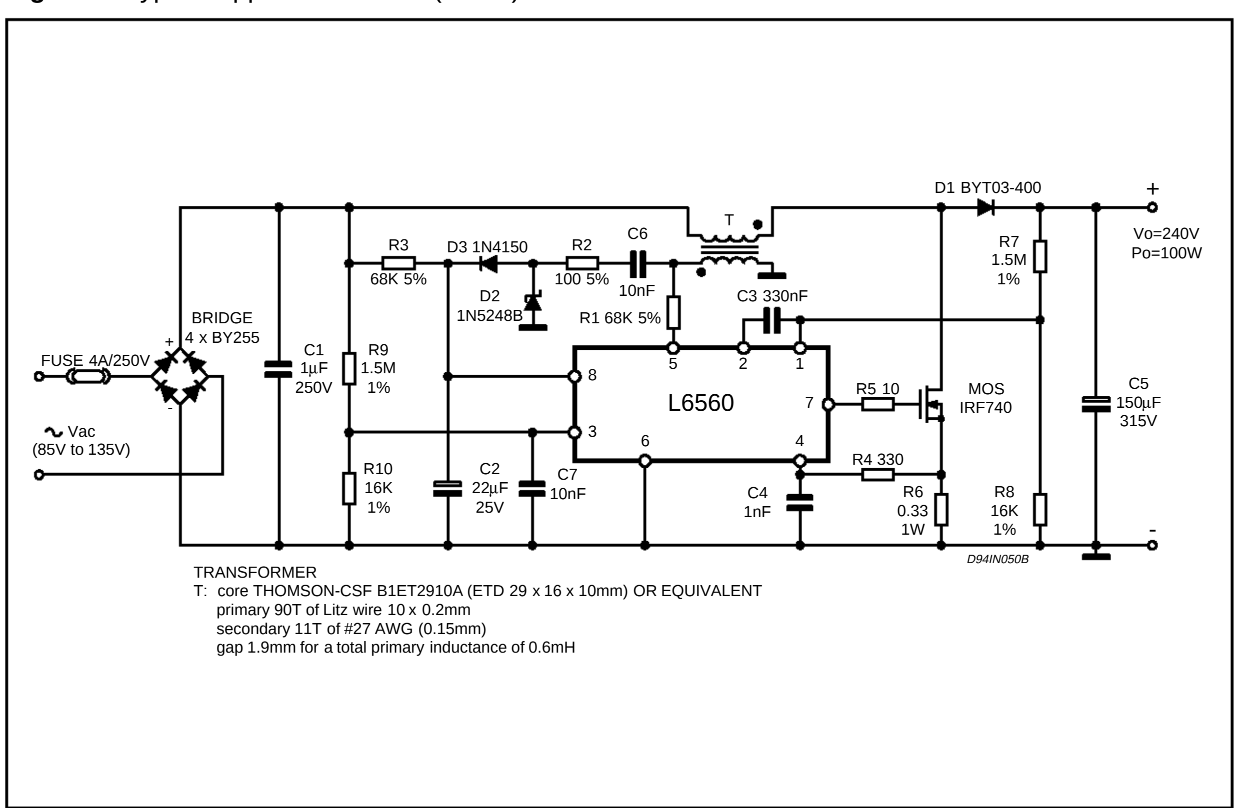


Figure 4: Typical Application Circuit (120W)

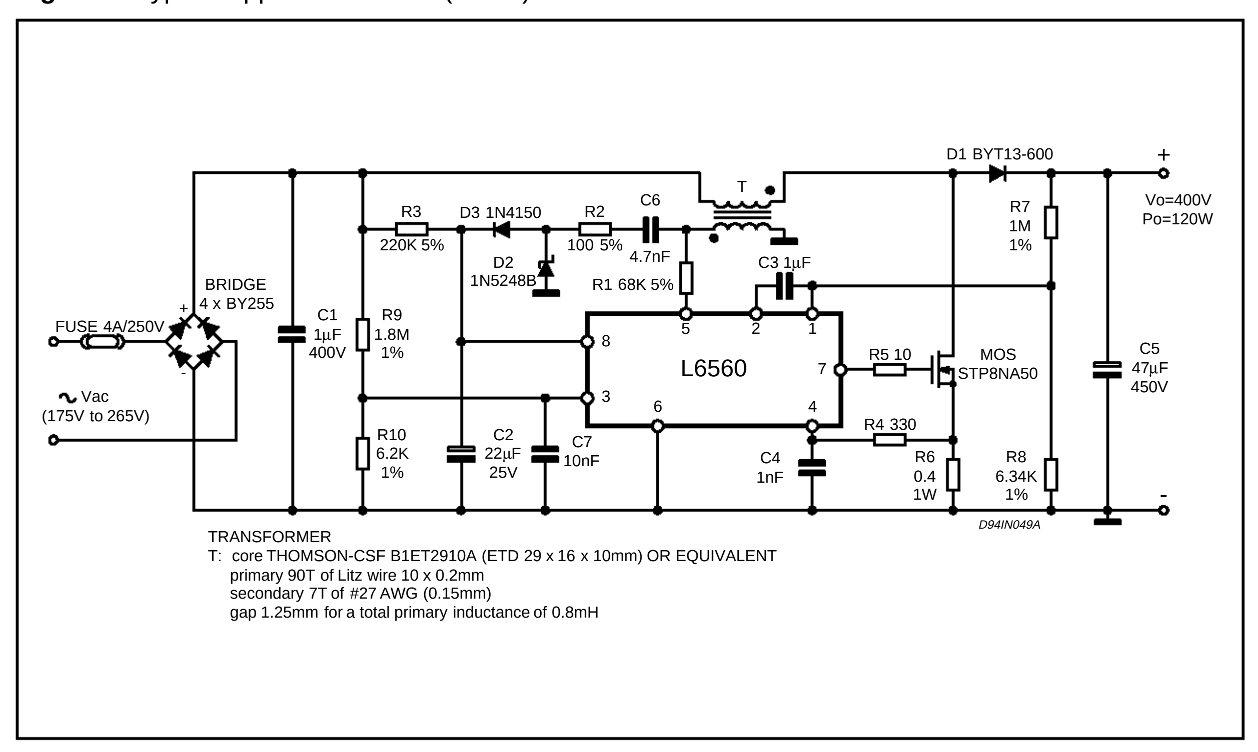


Figure 5: P.C. Board and Component Layout of the Figg. 3 and 4 (1:1.25 scale)

Figure 6: OVP Current Threshold vs. Temperature

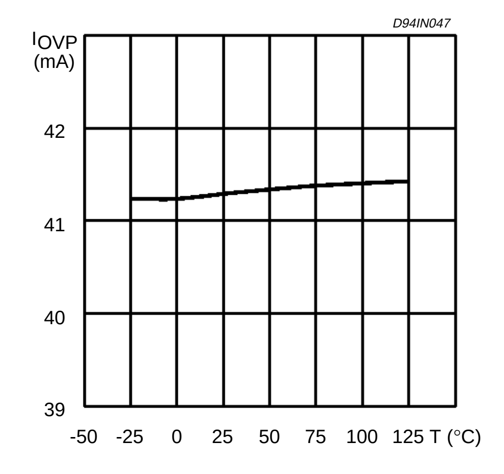


Figure 7: Undervoltage Lockout Threshold vs. Temperature

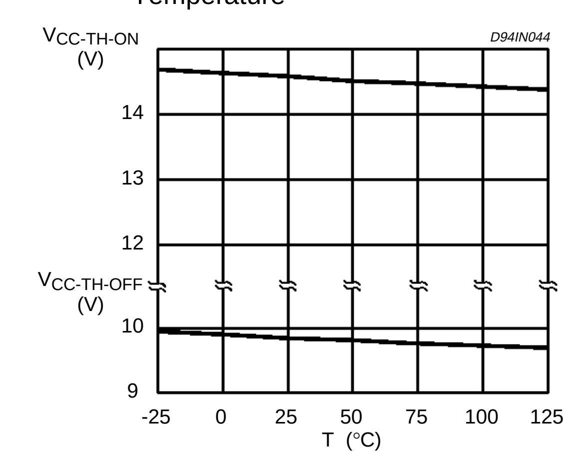


Figure 8: Supply Current vs. Supply Voltage

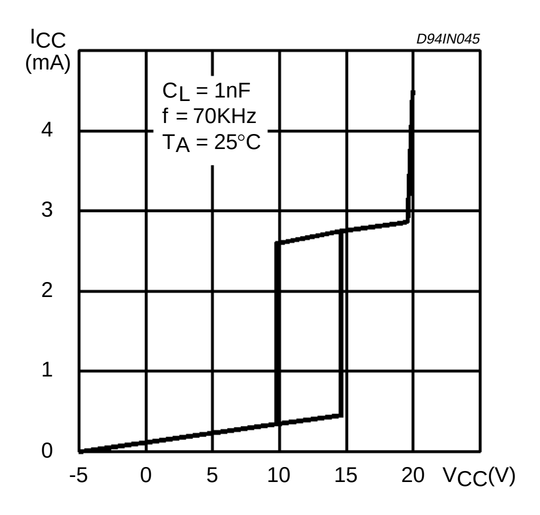


Figure 9: Voltage Feedback Input Threshold vs. Temperature

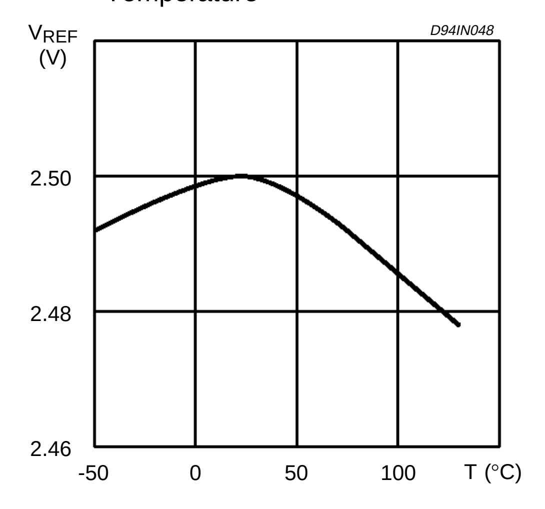


Figure 10: Output Saturation Voltage vs. Sink Current

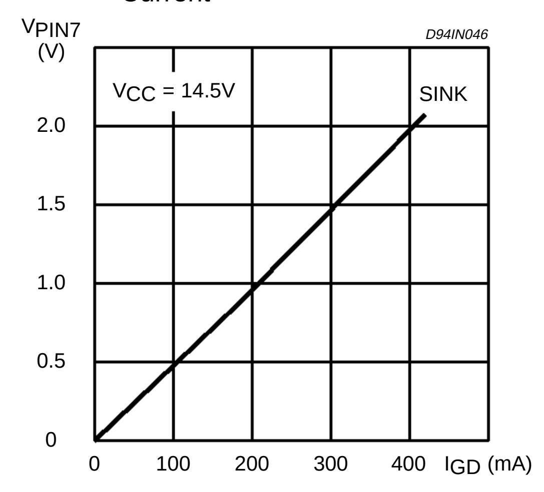


Figure 11: Output Saturation Voltage vs. Source Current

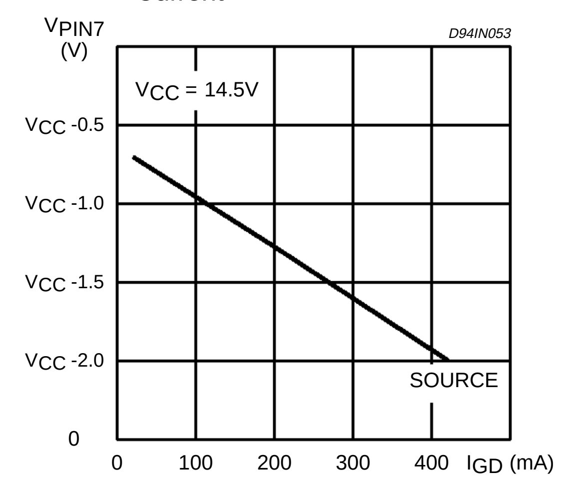


Figure 12: Multiplier Characteristics Family

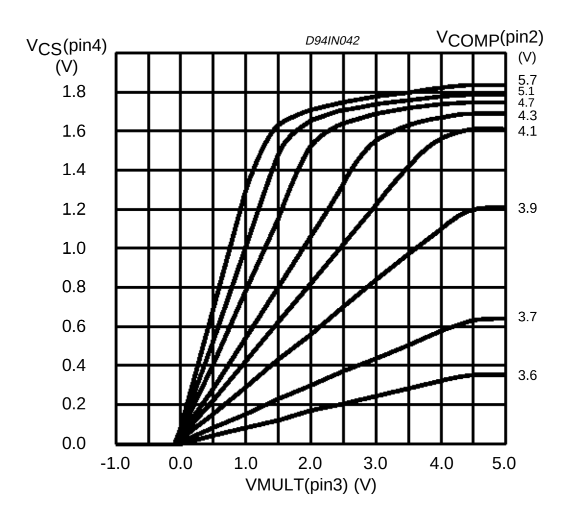
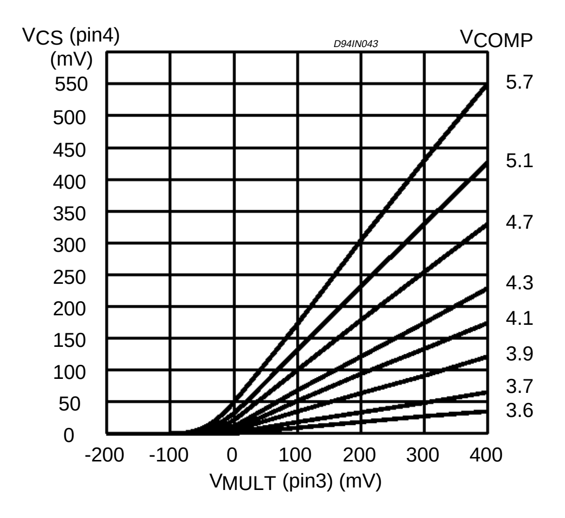
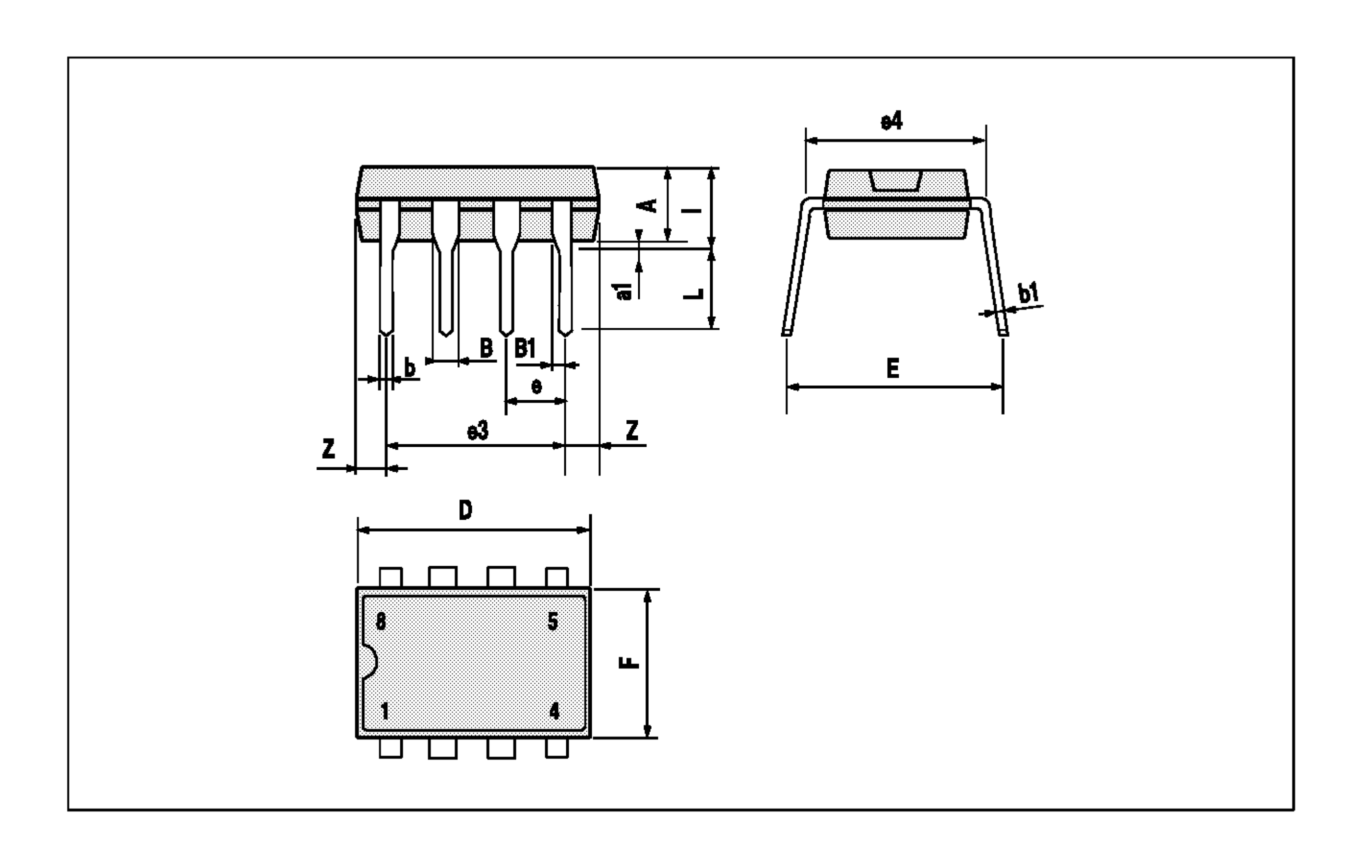


Figure 13: Multiplier Characteristics Family



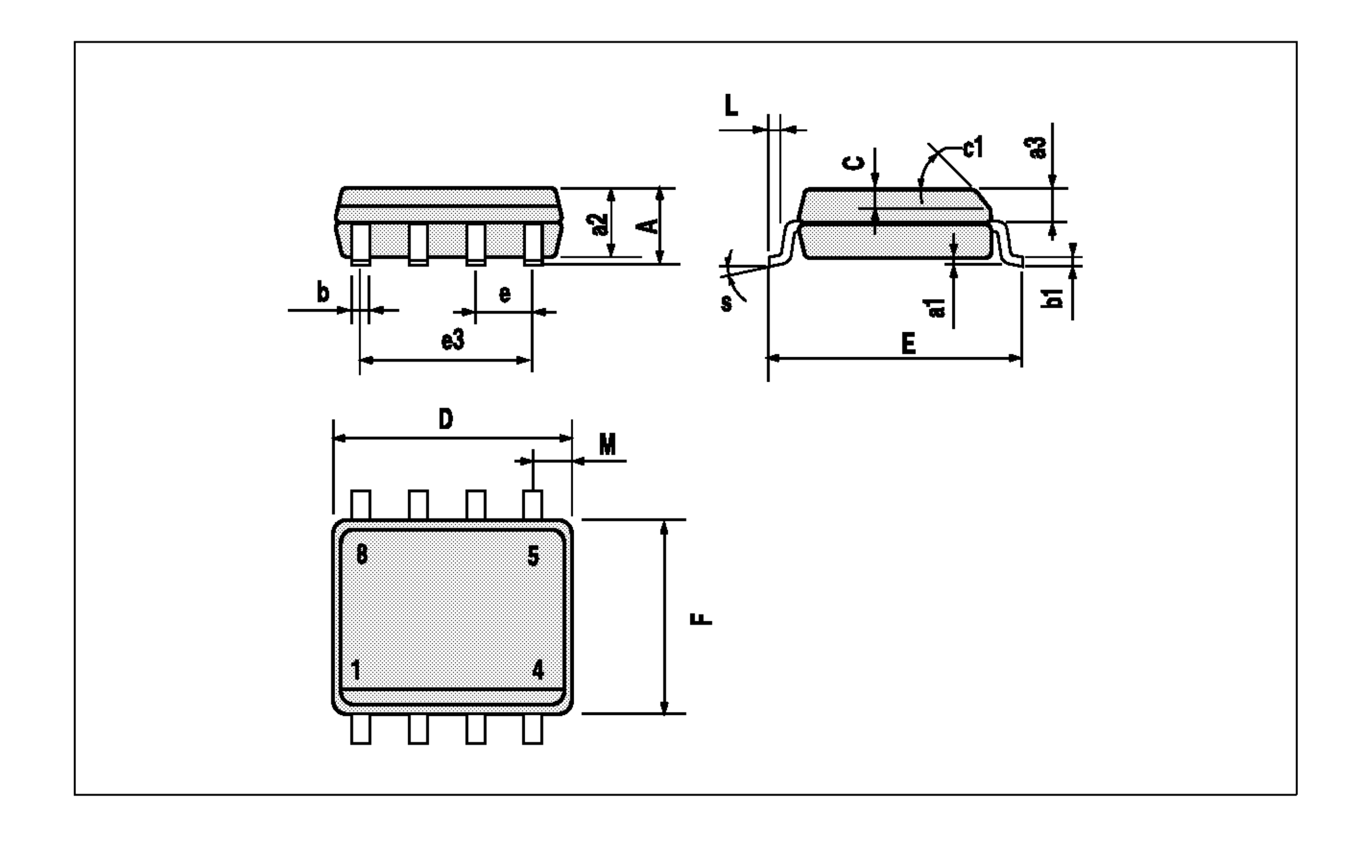
MINIDIP PACKAGE MECHANICAL DATA

DIM	mm			inch		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A		3.32			0.131	
a1	0.51			0.020		
B	1.15		1.65	0.045		0.065
b	0.356		0.55	0.014		0.022
b1	0.204		0.304	0.008		0.012
D			10.92			0.430
E	7.95		9.75	0.313		0.384
e		2.54			0.100	
e3		7.62			0.300	
e4		7.62			0.300	
F			6.6			0260
i			5.08			0.200
L	3.18		3.81	0.125		0.150
Z			1.52			0.060



SO8 PACKAGE MECHANICAL DATA

DIM	mm			inch		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.75			0.069
a1	0.1		0.25	0.004		0.010
a2			1.65			0.065
a3	0.65		0.85	0.026		0.033
b	0.35		0.48	0.014		0.019
b1	0.19		0.25	0.007		0.010
C	0.25		0.5	0.010		0.020
c1	45° (typ.)					
D	4.8		5.0	0.189		0.197
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		3.81			0.150	
F	3.8		4.0	0.150		0.157
L	0.4		1.27	0.016		0.050
M			0.6			0.024
S	8° (max.)					




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